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**PAT. & T.M. OFFICE
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AND INTERFERENCES**

Applicants: Evans, Jr. et al.
Serial No.: 07/582,672
Filed: 09/14/90
For: Non-Volatile Memory
Circuit Using Ferroelectric
Capacitor Storage Element

Accorded Benefit of: U.S. Serial Nos.
07/440,434 filed 10/20/89 and 07/057,100
filed 06/02/87, now abandoned

The case referred to above has been forwarded to the Board of Patent Appeals and Interferences because it is adjudged to interfere with other cases hereafter specified. Attention is directed to the fact that this interference is declared pursuant to 37 CFR 1.601 et seq., effective February 11, 1985 (49 F.R. 48416. 1050 O.G. 385). The interference is designated as No. 102,725.

By direction of the Commissioner of Patents and Trademarks and as required by 35 USC 135(c), notice is hereby given the parties of the requirement of the law for filing in the Patent and Trademark Office a copy of any agreement "in connection with or in contemplation of the termination of the interference."

The cases involved in this interference are:

Junior Party

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Serial No.: 07/582,672 filed 09/14/90

For: Non-Volatile Memory Circuit Using Ferroelectric Capacitor Storage Element

Assignees: National Semiconductor Corp., A Corp. of DE

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Accorded Benefit of: U.S. Serial Nos. 07/440,434 filed 10/20/89,
07/057,100 filed 06/02/87, now abandoned

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Serial No.: 07/013,746 filed 02/12/87, now Patent No. 4,873,664
issued 10/10/89

For: Self Restoring Ferroelectric Memory

Assignees: Ramtron Corporation, Colorado Springs, CO

Attorneys of Record: Ronald L. Wanke, Edward D. Manzo, James D. Ryndak, Jean M. Dudek and Roger R. Wise

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Accorded Benefit of: None

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Count 1

In a nonvolatile ferroelectric memory of the type having a plurality of memory cells, a bit line coupled to each said memory cell, each said memory cell comprising a ferroelectric capacitor having first and second plate electrodes, the polarization of said capacitors corresponding to the data stored therewithin, the improvement wherein:

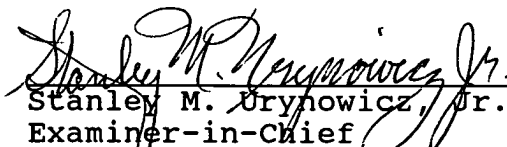
said memory further comprising a plurality of word lines and a plurality of plate lines distinct from said bit lines and word lines, each of the memory cells being coupled to a word line, each memory cell being coupled also to a plate line, each plate line being coupled to a capacitor plate electrode of a cell; and

each said memory cell further including a respective switching device located within the memory cell, said first plate electrode of said capacitor in said cell being coupled to one said bit line via said switching device, said switching device being coupled to be controlled by one said word line, said second plate electrode of said capacitor in said cell being coupled to one said plate line.

The claims of the parties which correspond to this count are:

Evans Jr., et al.: Claims 72-74

Eaton, Jr. : Claims 1 and 17


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